IN THE CLAIMS:

1-15. (Canceled)

16. (Previously presented) A load driving sample-and-hold amplification circuit, comprising:

a sampling circuit that carries out a sampling of an input signal; and

an operational amplifier that carries out an operational amplification of the input signal that has been subjected to the sampling by the sampling circuit,

wherein the operational amplifier includes:

first and second operational amplifier stages that are connected in this order in a series manner;

a first switch, provided between an output terminal of the first operational amplifier stage and an input terminal of the second operational amplifier stage, that connects or cuts off a connection of the first and second operational amplifier stages so as to be nonconductive in a first operation phase during which the sampling is carried out and so as to be conductive in a second operation phase during which the operational amplifier, as a whole, carries out the operational amplification;

a capacitor provided between an output terminal and the input terminal of the second operational amplifier stage; and

a second switch provided between the output terminal of the second operational amplifier stage and a load, means for causing the second switch to connect or cut off a

connection of the second operational amplifier stage and the load wherein the means causes the second switch to be conductive in the first operation phase and nonconductive in the second operation phase so that the second switch is conductive when the first switch is nonconductive, and vice versa, whereby driving time of amplification differs from drive time of the load so that low power consumption is realized.

17. (Previously presented) A sample-and-hold amplifier circuit, comprising:

a sampling circuit that carries out a sampling of an input signal; and

an operational amplifier that carries out an operational amplification of the input signal that has been subjected to the sampling by the sampling circuit,

wherein the operational amplifier includes:

first and second operational amplifier stages that are connected in this order in a series manner;

a switch, provided between an output terminal of the first operational amplifier stage and an input terminal of the second operational amplifier stage, that connects or cuts off a connection of the first and second operational amplifier stages so as to be nonconductive in a first operation phase during which the sampling is carried out and so as to be conductive in a second operation phase during which the operational amplifier, as a whole, carries out the operational amplification; and

a capacitor provided between an output terminal and the input terminal of the second operational amplifier stage;

wherein the operational amplifier includes: a resistor provided between the input and output terminals of the second operational amplifier stage so as to be connected with the capacitor in a series manner; and a second switch for short-circuiting the resistor, connected with the resistor in a parallel manner, that is conductive during the first operation phase and is nonconductive during the second operation phase.

18. (Previously presented) A load driving sample-and-hold amplification circuit, comprising:

a sampling circuit that carries out a sampling of an input signal; and

an operational amplifier that carries out an operational amplification of the input signal that has been subjected to the sampling by the sampling circuit,

wherein the operational amplifier includes:

multiple operational amplifier stages that are connected with each other in a series manner;

a first switch that: (a) connects or cuts off a connection of the operational amplifier stages, (b) is nonconductive during a first operation phase during which the sampling is carried out, and (c) is conductive in a second operation phase during which the operational amplification is carried out by the operational amplifier as a whole, said first switch being provided between neighboring first and second operational amplifier stages so as to be provided between an output terminal of the first operational amplifier stage and an input terminal of the second operational amplifier stage;

capacitors coupled to an output terminal of a final operational amplifier stage so that at least one of the capacitors is provided between the output terminal of the final operational amplifier stage and the input terminal of the second operational amplifier stage; and

a second switch provided between the output terminal of the final operational amplifier stage and a load, the second switch connecting or cutting off a connection of the final operational amplifier stage and the load so as to be conductive in the first operation phase and nonconductive in the second operation phase.

19. (Previously presented) The load driving sample-and-hold amplification circuit as set forth in claim 18,

wherein the operational amplifier includes:

resistors in communication with the output terminal of the final operational amplifier stage so as to be respectively connected with the capacitors in a series manner; and

a third switch for short-circuiting one of the resistors, the third switch being connected in a parallel manner with the one resistor and connected to one of the capacitors in a series manner, the third switch being conductive during the first operation phase and being nonconductive during the second operation phase.

20. (Previously presented) The load driving sample and hold amplification circuit as set forth in claim 16, wherein the operational amplifier further includes a resistor provided between the input and output terminals of the second operational amplifier stage so as to be connected with the capacitor in a series manner.

21. (Previously presented) A pipelined A/D converter, comprising:

first sub-A/D converter blocks, connected with each other in a series manner, that each directly receive a clock signal and include (a) a sub-A/D converter that converts an input signal into a predetermined-numbered bit information and (b) a sub-operational-circuit which converts the bit information into an analog value, carries out an operational amplification with respect to a difference between the analog value and the input signal so as to output the difference that has been subjected to the operational amplification, and

a second sub-A/D converter block that includes a sub-A/D converter which converts an output signal of the first sub-A/D converter block of a final stage into a remainder of the bit information,

said sub-operational-circuit being a sample-and-hold amplifier circuit that includes:

a sampling circuit that carries out a sampling of the input signal; and

an operational amplifier that carries out an operational amplification of the input signal that has been subjected to the sampling by the sampling circuit,

said operational amplifier including:

first and second operational amplifier stages that are connected in this order in a series manner;

a switch, provided between an output terminal of the first operational amplifier stage and an input terminal of the second operational amplifier stage, that connects or cuts off a connection of the first and second operational amplifier stages so as to be nonconductive in a first operation phase during which the sampling is carried out and so as to be conductive in a second operation phase during which the operational amplifier, as a whole, carries out the operational amplification; and

a capacitor provided between an output terminal and the input terminal of the second operational amplifier stage.

22. (Previously presented) The pipelined A/D converter as set forth in claim 21, wherein the operational amplifier further includes:

a resistor provided between the input and output terminals of the second operational amplifier stage so as to be connected with the capacitor in a series manner;

a second switch for short-circuiting the resistor, connected with the resistor in a parallel manner, that is conductive during the first operation phase and is nonconductive during the second operation phase.

23. (Previously presented) A pipelined A/D converter, comprising:

at least one first sub-A/D converter blocks, connected with each other in a series manner, wherein each of the at least one first sub-A/D converter block(s) include (a) a sub-A/D converter that converts an input signal into a predetermined-numbered bit information and (b) a sub-operational-circuit which converts the bit information into an analog value, carries out an operational amplification with respect to a difference between the analog value and the input signal so as to output the difference that has been subjected to the operational amplification , and

a second sub-A/D converter block that includes a sub-A/D converter which converts an output signal of the first sub-A/D converter block of the final stage into a remainder of the bit information,

said sub-operational-circuit being a sample-and-hold amplifier circuit that includes:

a sampling circuit that carries out a sampling of the input signal; and

an operational amplifier that carries out an operational amplification of the input signal that has been subjected to the sampling by the sampling circuit,

said operational amplifier including:

multiple operational amplifier stages that are connected with each other in a series manner;

a switch, that (a) connects or cuts off a connection of the operational amplifier stages, (b) is nonconductive during the first operation phase during which the sampling is

carried out, and (c) is conductive in the second operation phase during which the operational amplification is carried out by the operational amplifier as a whole, said switch being provided between neighboring first and second operational amplifier stages so as to be provided between an output terminal of the first operational amplifier stage and an input terminal of the second operational amplifier stage; and

capacitors operatively associated with an output terminal of a final operational amplifier stage so that at least one of the capacitors is provided between the output terminal of the final operational amplifier stage and at least the input terminal of the second operational amplifier stage.

24. (Previously presented) The pipelined A/D converter as set forth in claim 23, wherein the operational amplifier further includes:

resistors in communication with the output terminal of the final operational amplifier stage so as to be respectively connected with the capacitors in a series manner; and

another switch for short-circuiting a first one of the resistors, the another switch being connected in a parallel manner with said first one of resistors and connected to one of the capacitors in a series manner, the another switch being conductive during the first operation phase and being nonconductive during the second operation phase.

25. (Previously presented) The pipelined A/D converter as set forth in claim 21, wherein the operational amplifier further includes a resistor provided between the input and output terminals of the second operational amplifier stage so as to be connected with the capacitor in a series manner.

26. (Previously presented) A pipelined D/A converter, comprising:

a plurality of sample-and-hold amplifier circuits that are connected with each other in a series manner and each is used as a sub-D/A converter that converts a predetermined-numbered bit information of a digital signal into an analog value, each of the sample-and-hold circuits directly receiving a clock signal,

the sub-D/A converter carrying out an operational amplification with respect to an analog input signal and said analog value that corresponds to the predetermined-numbered bit information and sending the result of amplification to a sub-D/A converter of the next stage so that the sub-D/A converter of the final stage outputs an analog signal corresponding to the digital signal,

at least one of the sample-and-hold amplifier circuits including:

a sampling circuit that carries out a sampling of an input signal; and

an operational amplifier that carries out an operational amplification of the input signal that has been subjected to the sampling by the sampling circuit,

the operational amplifier including:

first and second operational amplifier stages that are connected in this order in a series manner;

a switch, provided between an output terminal of the first operational amplifier stage and an input terminal of the second operational amplifier stage, that connects or cuts off a connection of the first and second operational amplifier stages so as to be nonconductive in a first operation phase during which the sampling is carried out and so as to be conductive in a second operation phase during which the operational amplifier, as a whole, carries out the operational amplification; and

a capacitor provided between an output terminal and the input terminal of the second operational amplifier stage.

27. (Previously presented) The pipelined D/A converter as set forth in claim 26, wherein the operational amplifier includes:

a resistor provided between the input and output terminals of the second operational amplifier stage so as to be connected with the capacitor in a series manner;

a switch for short-circuiting the resistor, connected with the resistor in a parallel manner, that is conductive during the first operation phase and is nonconductive during the second operation phase.

28. (Previously presented) A pipelined D/A converter, comprising:

a plurality of sample-and-hold amplifier circuits that are connected with each other in a series manner and each is used as a sub-D/A converter that converts a predetermined-numbered bit information of a digital signal into an analog value,

the sub-D/A converter carrying out an operational amplification with respect to an analog input signal and said analog value that corresponds to the predetermined-numbered bit information and send the result of amplification to a sub-D/A converter of the next stage so that the sub-D/A converter of the final stage outputs an analog signal corresponding to the digital signal,

at least one of the sample-and-hold amplifier circuits including:

a sampling circuit that carries out a sampling of an input signal; and

an operational amplifier that carries out an operational amplification of the input signal that has been subjected to the sampling by the sampling circuit,

said operational amplifier including:

multiple operational amplifier stages that are connected with each other in a series manner;

a switch, that (a) connects or cuts off a connection of the operational amplifier stages, (b) is conductive during the first operation phase during which the sampling is carried out, and (c) is nonconductive in the second operation phase during which the operational amplification is carried out by the operational amplifier as a whole, said switch being provided between neighboring first and second operational amplifier stages

so as to be provided between an output terminal of the first operational amplifier stage and an input terminal of the second operational amplifier stage; and

capacitors coupled to an output terminal

of a final operational amplifier stage so that at least one of the capacitors is provided between the output terminal of the final operational amplifier stage and the input terminal of the second operational amplifier stage.

29. (Previously presented) The pipelined D/A converter as set forth in claim 28, wherein the operational amplifier includes:

resistors coupled to the output terminal of the final operational amplifier stage so as to be respectively connected with the capacitors in a series manner; and

another switch for short-circuiting one of the resistors, the another switch being connected in a parallel manner with the one resistor and wherein the another switch is conductive during the first operation phase and nonconductive during the second operation phase.

30. (Previously presented) The pipelined D/A converter as set forth in claim 26, wherein the operational amplifier further includes a resistor provided between the input and output terminals of the second operational amplifier stage so as to be connected with the capacitor in a series manner.

31. (Previously presented) The converter of claim 21, wherein the first and second amplifier stages are adjacent one another and are connected, and wherein each of the first and second amplifier stages receives the clock signal.

32. (Previously presented) The converter of claim 23, wherein the first and second amplifier stages are adjacent one another and are connected, and wherein each of the first and second amplifier stages receives the clock signal.

33. (Previously presented) The converter of claim 26, wherein the first and second amplifier stages are adjacent one another and are connected, and wherein each of the first and second amplifier stages receives the clock signal.

34. (Previously presented) The converter of claim 28, wherein the first and second amplifier stages are adjacent one another and are connected, and wherein each of the first and second amplifier stages receives the clock signal.

35. (Previously presented) A load driving sample-and-hold amplification circuit, comprising:

a sampling circuit that carries out a sampling of an input signal; and

an operational amplifier that carries out an operational amplification of the input signal that has been subjected to the sampling by the sampling circuit,

wherein the operational amplifier includes:

multiple operational amplifier stages that are connected with each other in a series manner;

a first switch that: (a) connects or cuts off a connection of the operational amplifier stages, (b) is nonconductive during a first operation phase during which the sampling is carried out, and (c) is conductive in a second operation phase during which the operational amplification is carried out by the operational amplifier as a whole, said first switch being provided between neighboring first and second operational amplifier stages so as to be provided between an output terminal of the first operational amplifier stage and an input terminal of the second operational amplifier stage;

capacitors coupled to an output terminal of a final operational amplifier stage so that at least one of the capacitors is provided between the output terminal of the final operational amplifier stage and the input terminal of the second operational amplifier stage;

a second switch provided between the output terminal of the final operational amplifier stage and a load, the second switch connecting or cutting off a connection of the final operational amplifier stage and the load so as to be conductive in the first operation phase and nonconductive in the second operation phase; and

wherein the operational amplifier further includes a resistor provided between the input and output terminals of the second operational amplifier stage so as to be connected with the capacitor in a series manner.

36. (Previously presented) The sample-and-hold amplifier circuit of claim 17, wherein the resistor is realized by an ON resistor of a transistor.

37. (Previously presented) The sample-and-hold amplification circuit of claim 19, wherein the resistor is realized by an ON resistor of a transistor.

38. (Previously presented) The sample-and-hold amplification circuit of claim 20, wherein the resistor is realized by an ON resistor of a transistor.

39. (Previously presented) The sample-and-hold amplification circuit of claim 35, wherein the resistor is realized by an ON resistor of a transistor.